Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-47 (Canceled)

48. (Previously presented) An integrated semiconductor structure comprising:

a multijunction solar cell including a first photoactive junction formed in a substrate forming a bottom subcell where there are no subcells located between the bottom subcell and the lower surface of the substrate, and a second photoactive junction formed in a region overlying said bottom subcell and forming a second subcell; and

means for passing current when said multijunction solar cell is shaded, wherein said means is on the same substrate as the multijunction solar cell, wherein said means and said bottom subcell have an identical sequence of semiconductor layers, wherein each semiconductor layer in the means has substantially the same composition and thickness as the corresponding layer in the bottom subcell, wherein the means for passing current is electrically connected in parallel across the multijunction solar cell.

49. (Previously presented) The structure as defined in claim 48, wherein said means for passing current is a bypass diode formed on the substrate.

50. (Previously presented) The structure as defined in claim 49, wherein said bottom subcell and said bypass diode are formed in the same process.

51. (Previously presented) The structure as defined in claim 49, wherein the bypass diode has a Schottky junction.

52. (Previously presented) An integrated semiconductor structure comprising:

a multijunction solar cell including a bottom subcell formed on a substrate where there are no subcells between the bottom subcell and the lower surface of the substrate;

and

means for passing current when said multijunction solar cell is shaded, wherein said means is on the same substrate as the multijunction solar cell, wherein said means and said bottom subcell have an identical sequence of semiconductor layers, wherein each semiconductor layer in the means has substantially the same composition and thickness as the corresponding layer in the bottom subcell, and wherein the means for passing current is electrically connected in parallel across the multijunction solar cell.

53. (Previously presented) The structure as defined in claim 52, wherein said bottom subcell is formed on a first portion of the substrate and said means for passing current is a bypass diode formed on a second portion of the substrate that is laterally spaced from said first portion.

54. (Previously presented) The structure as defined in claim 53, wherein said bottom subcell and said bypass diode are formed in the same process.

55. (Previously presented) The structure as defined in claim 53, wherein said bypass diode is electrically connected across the subcells of the multijunction solar cell to protect said subcells against reverse biasing.

56. (Previously presented) The structure as defined in claim 53 wherein the bypass diode has a Schottky junction.

57. (Previously presented) An integrated semiconductor structure comprising:

a multijunction solar cell including a first solar cell formed on a substrate; and

a bypass diode, on the same substrate as the solar cell, wherein the bypass diode is directly electrically connected to the base of said first solar cell and to a top cell of the multijunction solar cell for passing current when said multijunction solar cell is shaded, wherein said bypass diode and said first solar cell have an identical sequence of semiconductor layers, wherein each semiconductor layer in the bypass diode has substantially the same composition and thickness as the corresponding layer in the first solar cell; and further wherein

said first solar cell is the bottom solar cell where there are no solar cells between the first solar cell and the lower surface of the substrate.

58. (Previously presented) The structure as defined in claim 57, wherein said first solar cell is formed on a first portion of the substrate and said bypass diode is formed on a second portion of the substrate spaced apart from said first portion.

59. (Previously presented) The structure as defined in claim 57, further comprising a metal layer connecting said bypass diode to the base of the first solar cell.

60. (Previously presented) An integrated semiconductor structure comprising:

a multijunction solar cell including first and second solar cells on a substrate;

means for passing current when said multijunction solar cell is shaded; and

a deposited metal layer connecting said multijunction solar cell and said means for passing current, said deposited metal layer contained within said semiconductor structure and entirely on a surface of said means for passing current, wherein

one end of said metal layer is coupled to the base of said first solar cell and another end of said metal layer is coupled to one terminal of said means for passing current; and further wherein

said means for passing current and said first solar cell have an identical sequence of semiconductor layers, wherein each semiconductor layer in the means for passing current has substantially the same composition and thickness as the corresponding layer in the first solar cell, and wherein the metal layer is disposed on sides of layers between the base of the first solar cell and the terminal in the means for passing current.

61. (Previously presented) The structure as structure as defined in claim 60, wherein said first solar cell is formed on a first portion of the substrate, and said means for passing current is a bypass diode formed on a second portion of the substrate.

62. (Previously presented) The structure as defined in claim 60, wherein said multijunction solar cell and said means for passing current are separated by a trough, and said metal layer lies over said trough.

63. (Previously presented) The structure as defined in claim 60, wherein both said first solar cell and said bypass diode are formed in the same process.

64. (Previously presented) The structure as defined in claim 62, wherein said means for passing current is electrically connected across at least said first and second cells to protect said first and second cells against reverse biasing.

65. (Previously presented) A solar cell semiconductor device comprising:

an integral semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms the first cell of a multijunction solar cell; and

a second region laterally spaced apart from said first region and in which the sequence of layers corresponding to the sequence of layers forming said first cell forms a bypass diode to protect said multijunction solar cell against reverse biasing,

a metal layer entirely on a surface of the bypass diode and disposed in the space between the first and second region, wherein the metal layer electrically connects the bypass diode to the multijunction solar cell and electrically shorts a plurality of layers of the second region between the multijunction solar cell and the bypass diode, wherein

the sequence of semiconductor layers in the first region forming said first cell and the sequence of semiconductor layers in the second region forming said bypass diode are identical, wherein each semiconductor layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region.

66. (Previously Presented) A device as defined in claim 65, wherein the sequence of layers of said first cell and the sequence of layers of the bypass diode are formed in the same process step.

67. (Canceled)

68. (Previously presented) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of material deposited on said substrate, including a first region in which the sequence of layers of material forms at least one cell of a multijunction solar cell, and a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing, wherein the sequence of layers in the first region forming said at least one cell and the sequence of layers in the second region forming said bypass diode are

identical, wherein each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region; and

a first discontinuous lateral semiconductor conduction layer directly on said substrate wherein the first discontinuous lateral semiconductor conduction layer includes a first portion in the bypass diode that is adapted to electrically contact a metal layer disposed on a side of the discontinuous lateral conduction layer and a second portion in the bypass diode that is laterally spaced away from the first portion and adapted to electrically contact an active region of said bypass diode.

69. (Previously presented) A device as defined in claim 68, wherein said lateral conduction layer in the first region is physically separated from the lateral conduction layer in the second region.

70. (Previously presented) A device as defined in claim 68, wherein said lateral conduction layer is a highly doped layer.

71. (Previously presented) A device as defined in claim 70, wherein said lateral conduction layer is composed of GaAs.

72. (Previously presented) A device as defined in claim 68, wherein one of the layers of said sequence of layers is an etch stop layer, and a second lateral conduction layer is disposed directly over said etch stop layer.

73. (Previously presented) A device as defined in claim 68, wherein said substrate includes a photoactive junction.

74. (Previously presented) A device as defined in claim 73, wherein said substrate is germanium.

75. (Previously presented) A device as defined in claim 73, wherein said substrate forms an electrical connection path between said multijunction solar cell and said bypass diode.

76. (Previously presented) A device as defined in claim 68

wherein the metal layer is disposed on a portion of said substrate and over at least a portion of said second region and functioning to (i) electrically short layers of said second region, and (ii) connect the substrate to a second lateral conduction layer to complete the electrical circuit between the multijunction solar cell and the bypass diode.

77. (Previously presented) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell, and a second region in which the corresponding sequence of layers forms a bypass diode to protect said at least one cell of a multijunction solar cell against reverse

biasing, wherein the sequence of layers in the first region forming said at least one cell and the sequence of layers in the second region forming said bypass diode are identical, wherein each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region; and

a lateral conduction semiconductor layer deposited on said substrate including a first portion disposed in said first region, and a second portion disposed in said second region and physically separated from said first portion, wherein said second portion of said lateral conduction semiconductor layer includes a first region that directly and electrically contacts a first InGaP layer of said bypass diode and a second region laterally spaced apart from the first region that directly and electrically contacts a first metal layer.

78. (Previously presented) A device as defined in claim 77, wherein said lateral conduction layer is a highly doped layer.

79. (Previously presented) A device as defined in claim 77, wherein said lateral conduction layer is composed of GaAs.

80. (Previously presented) A device as defined in claim 77, wherein one of the layers of said sequence of layers is an etch stop layer, and said lateral conduction layer is disposed directly over said etch stop layer.

81. (Canceled)

82. (Previously presented) A device as defined in claim 77, wherein said bypass diode further comprises a GaAs layer disposed over said first InGaP layer, and a second InGaP layer disposed over said GaAs layer.

83. (Previously presented) A device as defined in claim 82, further comprising a second metal layer deposited over said second InGaP layer and forming a Schottky junction with said second InGaP layer.

84. (Previously presented) A device as defined in claim 77, wherein said substrate includes a photoactive junction.

85. (Previously presented) A device as defined in claim 77 wherein said substrate is germanium.

86. (Previously presented) A device as defined in claim 77, wherein said substrate forms an electrical connection path between said multijunction solar cell and said bypass diode.

87. (Previously presented) A device as defined in claim 86, wherein the first metal layer is disposed on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

88. (Previously presented) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell;

a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing, wherein the sequence of layers in the first region forming said at least one cell and the sequence of layers in the second region forming said, bypass diode are identical, wherein each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region; and

wherein said sequence of layers includes a highly conductive discontinuous lateral semiconductor conduction layer deposited on said substrate

and wherein the discontinuous lateral semiconductor conduction layer includes a first portion in the bypass diode for making direct electrical contact with a first active layer of said bypass diode and a second portion in the bypass diode laterally spaced away from the first portion and adapted to form a contact region beneath the active layer to allow said bypass diode to be electrically connected to said multijunction solar cell.

89. (Previously presented) A device as defined in claim 88, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and

functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

90. (Previously presented) A device as defined in claim 88, wherein said lateral conduction layer includes a first portion disposed in said first region, and a second portion disposed in said second region and separated from the first portion.

91. (Previously presented) A device as defined in claim 88, wherein said lateral conduction layer is a highly doped layer composed of GaAs.

92. (Previously presented) A device as defined in claim 90, wherein said second portion of said lateral conduction layer makes electrical contact with the first active layer of said bypass diode.

93. (Previously presented) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell;

a second region laterally spaced apart from said first region, wherein the sequence of layers in said second region and the sequence of layers in said first region are identical, wherein

each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region; and

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting semiconductor layers between the substrate and a lateral conduction semiconductor layer of said second region to enable a bypass diode to be formed in said second region, said metal layer contained within said solar cell semiconductor device.

94. (Previously presented) A device as defined in claim 93,

wherein said metal layer connects said multijunction solar cell and said bypass diode with one end of said metal layer being coupled to the base of said one solar cell and another end of said metal layer is coupled to one terminal of said bypass diode.

95. (Previously presented) A device as defined in claim 93, wherein said first portion and said second portion are separated by a trough, and said metal layer lies over at least a portion of said trough.

96. (Previously presented) A device as defined in claim 93, wherein at least one layer of said first solar cell and said bypass diode are simultaneously formed in the same process.

97. (Previously presented) A device as defined in claim 93, wherein said bypass diode is electrically connected by said metal layer across said solar cell to protect said solar cell against reverse biasing.

98. (Previously presented) A device as defined in claim 93

the lateral conduction layer is on said substrate and electrically connects the multijunction solar cell to said bypass diode.